Solving Linear and Quadratic Programs with an Analog Circuit

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Abstract

We present the design of an analog circuit which solves linear programming (LP) or Quadratic Programming (QP) problems. In particular, the steady-state circuit voltages are the components of the LP (QP) optimal solution. The paper shows how to construct the circuit and provides a proof of equivalence between the circuit and the LP (QP) problem. The proposed method is used to implement a LP-based Model Predictive Controller by using an analog circuit. Simulative and experimental results show the effectiveness of the proposed approach.

Keywords: optimization, MPC, linear programming, quadratic programming, analog computation, linear complementarity systems

1. Introduction

Analog circuits for solving optimization problems have been extensively studied in the past [1, 2, 3]. Our renewed interests stems from Model Predictive Control (MPC) [4], [5]. In MPC at each sampling time, starting at the current state, an open-loop optimal control problem is solved over a finite horizon. The optimal command signal is applied to the process only during the following sampling interval. At the next time step a new optimal control problem based on new measurements of the state is solved over a shifted horizon. The optimal solution relies on a dynamic model of the process, respects input and output constraints, and minimizes a performance index. When the model is linear and the performance index is based on two-norm, one-norm or ∞-norm, the resulting optimization problem can be cast as a linear program (LP) or a quadratic program (QP), where the state enters the right hand side (rhs) of the constraints.

We present the design of an analog circuit whose steady state voltages are the LP/QP optimizers. Thevenin Theorem is used to prove that the proposed design yields a passive circuit. Passivity and KKT conditions of a tailored Quadratic

Program are used to prove that the analog circuit solves the associated LP or QP. The proposed analog circuit can be used to repeatedly solve LPs or QPs with varying rhs and therefore is suited for linear MPC controller implementation. For some classes of applications the suggested implementation can be faster, cheaper and consume less power than digital implementation. A comparison to existing literature reveals that the proposed circuit is simpler and faster than previously published designs.

The paper is organized as follows. Existing literature is discussed in section 2. We show how to construct an analog circuit from a given LP in section 3. Section 4 proves the equivalence between the LP and the circuit. Section 6 shows how to extend the LP results to solve QP problems. Simulative and experimental results show the effectiveness of the approach in section 7. Concluding remarks are presented in section 8.

2. Previous Work on Analog Optimization

2.1. Optimization problems and electrical networks

Consider the linear programming (LP) problem

$$\min_{V=[V_1,\ldots,V_n]} c^T V \tag{1a}$$

$$\text{s.t.} \quad A_{\text{eq}} V = b_{\text{eq}} \tag{1b}$$

$$A_{\text{ineq}} V \leq b_{\text{ineq}} \tag{1c}$$

where $[V_1, \ldots, V_n]$ are the optimization variables, A_{ineq} and A_{eq} are matrices, and c, b_{eq} and b_{ineq} are column vectors.

The monogram by J. Dennis [1] from 1959 presents an analog electrical network for solving the LP (1). In Dennis's work the primal and dual optimization variables are represented by the circuit currents and voltages, respectively. A basic version of Dennis's circuit consists of resistors, current sources, voltage sources and diodes. In this circuit each entry of matrices A_{ineq} and A_{eq} is equal to number of wires that are connected to a common node. Therefore, this circuit is limited to problems where the matrices A_{ineq} and A_{eq} contain only small integer values. An extended version of the circuit includes multiport DC-DC transformer and can represent arbitrary matrices A_{ineq} and A_{eq}. Current distribution laws in electrical networks (also known as minimum dissipation of energy principle or Kirchoff's laws) are used to prove that the circuit converges to the solution of the optimization problem. This work had limited practical impact due to difficulties in implementing the circuit, and especially in implementing the multiport DC-DC transformer.

In later work, Chua [6] showed a different and more practical way to realize the multiport DC-DC transformer using operational amplifiers. In subsequent works, Chua [3], [7] and Hopefield [2] proposed circuits to solve non-linear op-

timization problem of the form

$$\begin{aligned} &\min_x \ f(x) \\ &\text{s.t. } g_j(x) \leq 0, \ j = 1 \dots m \end{aligned} \tag{2}$$

where $x \in \mathbb{R}^n$ is vector of optimization variables, $f(x)$ is the cost function and $g_j(x)$ are the m constraint functions. The LP (1) was solved as a special case of problem (2) [3], [2]. The circuits proposed by Chua, Hopefield and coauthors model the Karush-Kuhn-Tucker (KKT) conditions by representing primal variables as capacitor voltages and dual variables as currents. The dual variables are driven by the inequality constraint violations using high gain amplifiers. The circuit is constructed in a way that capacitors are charged with a current proportional to the gradient of the Lagrangian of problem (2)

$$\frac{\partial x_i}{\partial t} = - \left[\frac{\partial f(x)}{\partial x_i} + \sum_{j=1}^{m} I_j \frac{\partial g_j(x)}{\partial x_i} \right] \tag{3}$$

where $\frac{\partial x_i}{\partial t}$ is the capacitor voltage derivative and I_j is the current corresponding to the j-th dual variable. The derivatives $\frac{\partial f}{\partial x_i}$ and $\frac{\partial g_j}{\partial x_i}$ are implemented by using combinations of analog electrical devices [8]. When the circuit reaches an equilibrium, the capacitor charge is constant ($\frac{\partial x_i}{\partial t} = 0$) and equation (3) becomes one of the KKT conditions. The authors prove that their circuit always reaches an equilibrium point that satisfies the KKT conditions. This is an elegant approach since the circuit can be intuitively mapped to the KKT equations. However, the time required for the capacitors to reach an equilibrium is non-negligible. This might be the reason for relatively large settling time reported to be "tens of milliseconds" for those circuits in [3].

2.2. Applying analog circuits to MPC problems

The analog computing era declined before the widespread use of Model Predictive Control. Quero, Camacho and Franquelo in [9] have been the first to study the implementation of analog MPC. They use the Hopfield circuit proposed in [2] to implement an MPC controller. The approach they propose is validated with an experimental circuit which reaches the equilibrium after a transient of 1.8 msec.

More recently in [10] fast analog PI controllers are implemented on an Anadigm's Field Programmable Analog Array (FPAA) device [11] for an application involving fast chemical microreactor. The analog circuit designed in [10] has a computation time faster than a digital controller implementing the PI controller. The article briefly proposes to use FPAA for MPC without specifying details. To the best of authors knowledge, no further work has been published in this direction.

Figure 1: A node with k connected wires

Figure 2: Equality enforcing circuit. Consists of n resistors R_k, a negative resistance and a reference voltage.

3. LP Analog Circuit

Without loss of generality, we assume that A_{ineq}, A_{eq} and c have non-negative entries. Any LP may be transformed into this form by using a three-step procedure. First, defining a new negative and positive variable for each original variable $V^- + V^+ = 0$, second splitting A_{ineq}, A_{eq} and c into positive and negative parts ($A_{\text{ineq}} = A^+_{\text{ineq}} - A^-_{\text{ineq}}$, $A_{\text{eq}} = A^+_{\text{eq}} - A^-_{\text{eq}}$ and $c = c^+ - c^-$), and third replacing $A_{\text{ineq}}V$, $A_{\text{eq}}V$ and c^TV with $A^+_{\text{ineq}}V^+ + A^-_{\text{ineq}}V^-$, $A^+_{\text{eq}}V^+ + A^-_{\text{eq}}V^-$ and ${c^+}^T V^+ + {c^-}^T V^-$, respectively.

In the beginning of this section we present the basic building blocks which will be lately used to create a circuit that solves problem (1). The first basic block enforces equality constraints of the form (1b). The second building block enforces inequality constraints of the form (1c). The last basic block implements the cost function.

3.1. Equality constraint

Consider the circuit depicted in Fig. 1. In this circuit n wires are connected to a common node. We call this common node α, its potential is U and the current that exits this node is I. Kirchhoff's current law (KCL) implies

$$\sum_{k=1}^{n} I_k = \sum_{k=1}^{n} \frac{V_k - U}{R_k} = I, \tag{4}$$

where V_k is the potential of node k, R_k is the resistance between node k and the node α. Equation (4) can be written as an equality constraint on potentials V_k:

$$\sum_{k=1}^{n} \frac{V_k}{R_k} = I + U \sum_{k=1}^{n} \frac{1}{R_k}. \tag{5}$$

If we can set the right hand side (rhs) of (5) to any desired value b, then (5) enforces an equality constraint on a linear combinations of V_k. Therefore every equality constraint (1b) can be implemented with a circuit which enforces (5) and implements

$$U = \frac{b - I}{\sum_{k=1}^{n} \frac{1}{R_k}}. \tag{6}$$

Figure 3: Inequality enforcing circuit.

Equation (6) together with (5) yields

$$\begin{bmatrix} \frac{1}{R_1} & \cdots & \frac{1}{R_n} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} = b. \tag{7}$$

and the circuit implementing (7) is shown in Fig. 2.

Remark 1. *In the circuit in Fig. 2 the negative resistance* $-\frac{1}{\sum_k \frac{1}{R_k}}$ *can be realized by using operational amplifier.*

3.2. Inequality constraint

Consider the circuit shown in Fig. 3. Similarly to the equality constraint circuit, n wires are connected to a common node α. Its potential is U and the current exiting this node is I. Kirchhoff's current law (KCL) implies

$$\sum_{k=1}^{n} I_k = \sum_{k=1}^{n} \frac{V_k - U}{R_k} = I. \tag{8}$$

An ideal diode connects node α to node β. The potential of node β is U'. The diode enforces $U \leq U'$. In Fig. 3, the voltage U' can be computed as follows

$$U' = \frac{b - I}{\sum_{k=1}^{n} \frac{1}{R_k}} \geq U. \tag{9}$$

Equation (8) and $U \leq U'$ yield

$$\sum_{k=1}^{n} \frac{V_k}{R_k} = I + U \sum_{k=1}^{n} \frac{1}{R_k} \leq I + U' \sum_{k=1}^{n} \frac{1}{R_k} = b. \tag{10}$$

Which can be compactly rewritten as

$$\begin{bmatrix} \frac{1}{R_1} & \cdots & \frac{1}{R_n} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} \leq b, \tag{11}$$

with the diode enforcing

$$I \geq 0, \tag{12a}$$

$$I(U - U') = 0. \tag{12b}$$

By using (9) and rearranging its terms, equation (12b) can be rewritten as:

$$I \left(\left(\sum_{k=1}^{n} \frac{1}{R_k} \right) U - b + I \right) = 0. \tag{13}$$

Figure 4: Cost circuit

Figure 5: Electric Circuit solving an LP. Vertical wires are variable nodes with potentials $V_1 \dots V_n$. Black dots represent resistances that connects vertical and horizontal wires. Horizontal wires are cost or constraint nodes. Each horizontal wire is connected to a ground via a negative resistance, a constant voltage source and a diode for inequalities nodes. The topmost horizontal wire is the cost circuit which is connected to a constant voltage source.

3.3. Cost function

Consider the circuit in Fig. 4. In this circuit the potential of node α is equal to U_{cost} and the current that exits the node is I_{cost}. From (5) we have

$$c^T V = I_{\text{cost}} + U_{\text{cost}} \sum_{k=1}^{n} \frac{1}{R_k} \triangleq J. \tag{14}$$

where $c = [1/R_1 \ \dots \ 1/R_n]$, $V = [V_1 \ \dots \ V_n]$ and J is the cost function.

This part of the circuit implements the minimization of the cost function. When U_{cost} is set to a low value, the voltages V_k are driven to a direction which forces the cost J to approach the U_{cost} value. However, the cost J is different from U_{cost} because the current I_{cost} is not zero. A detailed explanation on this part of the circuit will be presented later in section 4.2.

3.4. Connecting the basic circuits

This section presents how to construct the circuit that solves a general LP. We construct the conductance matrix $G \in \mathbb{R}^{(m+1)\times n}$ as

$$G \triangleq \begin{bmatrix} c^T \\ A \end{bmatrix} = \begin{bmatrix} c^T \\ A_{\text{eq}} \\ A_{\text{ineq}} \end{bmatrix} \tag{15}$$

and denote G_{ij} the i, j element of G. For a given LP (1) the R_{ij} resistor is defined as

$$R_{ij} = \frac{1}{G_{ij}}, \ i = 0, \dots m, \quad j = 1, \dots, n \tag{16}$$

where the first row of G (corresponding to c^T) is indexed by 0.

Consider the circuit shown in Fig. 5. The circuit is shown using a compact notation where each resistor R_{ij} is represented by a dot, vertical wires represent variables nodes with potentials $V_1 \dots V_n$ and horizontal wires represent *constraint nodes*. The compact representation of a resistor through the dot symbol is clarified in Fig. 6. If $G_{ij} = 0$ then no resistor is present in the corresponding dot.

The LP circuit is constructed by connecting the nodes associated with the variables $V_1 \dots V_n$ to all three types of the basic circuits: equality, inequality

Figure 6: Compact representation of a resistor.

and cost. We will refer to such nodes as *variable nodes*. Each row of the circuit in Fig. 5 is one of the basic circuits presented in Sections 3.1, 3.2 and 3.3. We claim that, if U_{cost} is "small enough", then the values of the potentials $V_1 \dots V_n$ in this circuit are a solution of (1). This claim is proven in the next section.

Remark 2. *Some of the potentials V_i may be forced externally to a desired value. By doing so, the circuit can solve different optimization problems for varying values of those potentials. This is equivalent to adding equality constraints $V_i = b_i$ to* (1) *and modifying the value of the equality constraint free parameter b_i.*

Remark 3. *The circuit as shown in Fig. 5 contains no dynamic elements such as capacitor or inductance. Therefore, the time required to reach steady-state is governed by the parasitic effects (e.g. wires inductance and capacitance) and by the properties of the elements used to realize negative resistance (usually opamp) and diode. Hence, a good electronic design can achieves solution times in the order of these parasitic effects. This could lead to time constants as low as a few nanoseconds.*

4. Steady-State Analysis of the LP Circuit

Consider the LP circuit in Fig. 5 with R_{ij} defined by equations (15)-(16). In this section we show that there exists a range of U_{cost} values such that the LP circuit in Fig. 5 solves the optimization problem (1). In particular, the steady-state circuit voltages are the components of an LP optimal solution. First, we derive the steady state equations of the electric circuit and then we show the equivalence.

4.1. Steady state solution

Consider the circuit in Fig. 5. Let $U = [U_1, \dots, U_m]^T$ be the voltages of the constraint nodes as shown on Fig. 5. By applying the KCL (Kirchhoff's current law) to every variable node with potential $V_1, \dots, V_n$ we obtain

$$G_{0,j}(U_{\text{cost}} - V_j) + \sum_{i=1}^{m} G_{i,j}(U_i - V_j) = 0, \quad j = 1, \dots, n \tag{17}$$

which can be rewritten in the matrix form

$$\begin{bmatrix} c_1 & . & c_n \\ A_{11} & . & A_{1n} \\ \vdots & . & \vdots \\ A_{m1} & . & A_{mn} \end{bmatrix}^T \begin{bmatrix} U_{\text{cost}} \\ U_1 \\ \vdots \\ U_m \end{bmatrix} = \begin{bmatrix} (\sum_{i=0}^{m} G_{i,1})V_1 \\ \vdots \\ (\sum_{i=0}^{m} G_{i,n})V_n \end{bmatrix}, \tag{18}$$

Equation (18) can be compactly written as

$$cU_{\text{cost}} + A^T U = \text{diag}(c^T + \mathbf{1}^T A)V \tag{19}$$

where m is the number of equality and inequality constraints, $\mathbf{1}$ is a vector of ones and $\text{diag}(x)$ is a diagonal matrix with x on its diagonal.

Next, we apply KCL on all nodes with potentials $[U_{\text{cost}}, U_1, \ldots, U_m]$ to obtain

$$\sum_{j=1}^{n} c_j(U_{\text{cost}} - V_j) = I_{\text{cost}} \tag{20}$$

$$\sum_{j=1}^{n} G_{i,j}(U_i - V_j) = I_i, \qquad i = 1, \ldots, m \tag{21}$$

which can be written in matrix form

$$\begin{bmatrix} c_1 & . & c_n \\ A_{11} & . & A_{1n} \\ \vdots & . & \vdots \\ A_{m1} & . & A_{mn} \end{bmatrix} \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} = \begin{bmatrix} U_{\text{cost}} \sum_{j=1}^{n} c_j \\ U_1 \sum_{j=1}^{n} A_{1,j} \\ \vdots \\ U_m \sum_{j=1}^{n} A_{m,j} \end{bmatrix} + \begin{bmatrix} I_{\text{cost}} \\ I \end{bmatrix}, \tag{22}$$

where $I = [I_1 \ \ldots \ I_n]$. Equation (22) can be compactly rewritten as

$$c^T V = \mathbf{1}^T c U_{\text{cost}} + I_{\text{cost}} \tag{23a}$$

$$AV = \text{diag}\left(\mathbf{1}^T A^T\right) U + I. \tag{23b}$$

The equality voltage regulator law (6) and the inequality law (9) can be compactly written as

$$\text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}} = b_{\text{eq}} - I_{\text{eq}} \tag{24a}$$

$$\text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}} \leq b_{\text{ineq}} - I_{\text{ineq}}. \tag{24b}$$

By substituting (24) into (23b) we obtain

$$A_{\text{eq}} V = b_{\text{eq}} \tag{25a}$$

$$A_{\text{ineq}} V \leq b_{\text{ineq}}. \tag{25b}$$

Substitution of (23b) for inequalities to the diode constraint (13) yields

$$\left[A_{\text{ineq}} V - b_{\text{ineq}}\right]_i \left[I_{\text{ineq}}\right]_i = 0, \ \forall i \in \mathcal{I} \tag{26}$$

where $\mathcal{I}$ is the set of all inequalities constraints.

We collect (19), (23), (25) and (12a) into one set of equations which characterize the circuit

$$AV = \operatorname{diag}\left(\mathbf{1}^T A^T\right) U + I \tag{27a}$$
$$cU_{\text{cost}} + A^T U = \operatorname{diag}(c^T + \mathbf{1}^T A)V \tag{27b}$$
$$A_{\text{eq}} V = b_{\text{eq}} \tag{27c}$$
$$A_{\text{ineq}} V \leq b_{\text{ineq}} \tag{27d}$$
$$I_{\text{ineq}} \geq 0 \tag{27e}$$
$$\left[A_{\text{ineq}} V - b_{\text{ineq}}\right]_i \left[I_{\text{ineq}}\right]_i = 0, \forall i \in \mathcal{I} \tag{27f}$$
$$c^T V = \mathbf{1}^T c U_{\text{cost}} + I_{\text{cost}}, \tag{27g}$$

where U, I, I_{cost} and V are the unknowns. The voltage U_{cost} of the cost node is set externally.

4.2. Equivalence of the optimization problem and the electric circuit

We consider the following assumptions.

Assumption 1. *The LP* (1) *is feasible and the feasible set is bounded.*

Assumption 2. *The dual of LP* (1) *is feasible and the set of dual optimal solutions is bounded.*

Assumption 3. *In the LP* (1)*, G is non-negative, $\mathbf{1}^T G > 0$ and $\mathbf{1}^T G^T > 0$.*

Theorem 1 (circuit equivalence)**.** *Let Assumptions 1-3 hold. Then, there exists U_{cost}^{crit}, such that a solution V^* to* (27) *is also an optimizer of the LP* (1) *for all $U_{cost} \leq U_{cost}^{crit}$.*

Theorem 1 will be proven in the following way: first we claim that the equations (27a)-(27f) have a solution when the cost function is not present ($c = 0$); second, we show that there exists $U_{\text{cost}}^{\text{crit}}$ such that any solution to (27) is also an LP solution; third, we show that for all $U_{\text{cost}} \leq U_{\text{cost}}^{\text{crit}}$ any solution to (27) is also an LP solution.

Remark 4. *As explained earlier in this paper, the assumption on the non-negativity of G in Theorem 1 is not restrictive. Also, $\mathbf{1}^T G > 0$ and $\mathbf{1}^T G^T > 0$ are always satisfied for LP problems without zero rows or zero columns.*

Remark 5. *In Theorem 1 we require that the sets of primal optimal and dual optimal solutions are bounded. This can be guaranteed if the primal feasible set is bounded and linear independent constraint qualification (LICQ) holds.*

Consider an electric circuit with constraint sub circuits and no cost sub circuit. Such an electric circuit is characterized by (27a)-(27f) with $c = 0$.

Lemma 1 (Existence of solution to a zero-cost circuit)**.** *Let Assumption 1 hold. Assume that A is non-negative, $\mathbf{1}^T A > 0$ and $\mathbf{1}^T A^T > 0$. Then, the equations (27a)-(27f) have a solution when $c = 0$.*

Proof. First we rearrange (27a)-(27f). Equation (27a) can be split into an equality and inequality parts

$$A_{\text{eq}} = \text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}} + I_{\text{eq}} \tag{28}$$
$$A_{\text{ineq}} = \text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}} + I_{\text{ineq}}. \tag{29}$$

Equation (27b) can be rewritten as

$$A_{\text{eq}}^T U_{\text{eq}} + A_{\text{ineq}}^T U_{\text{ineq}} = \text{diag}\left(\mathbf{1}^T A\right) V. \tag{30}$$

Therefore, (27a)-(27f) can be written as

$$A_{\text{eq}} V = \text{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U_{\text{eq}} + I_{\text{eq}} \tag{31a}$$
$$A_{\text{ineq}} V = \text{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U_{\text{ineq}} + I_{\text{ineq}} \tag{31b}$$
$$A_{\text{eq}}^T U_{\text{eq}} + A_{\text{ineq}}^T U_{\text{ineq}} = \text{diag}\left(\mathbf{1}^T A\right) V \tag{31c}$$
$$A_{\text{eq}} V = b_{\text{eq}} \tag{31d}$$
$$A_{\text{ineq}} V \leq b_{\text{ineq}} \tag{31e}$$
$$I_{\text{ineq}} \geq 0 \tag{31f}$$
$$\left(A_{\text{ineq}} V - b_{\text{ineq}}\right)_i I_{\text{ineq}_i} = 0, \ \forall i \in \mathcal{I}. \tag{31g}$$

Next, consider the following quadratic program (QP)

$$\begin{aligned} \min_V \ & \frac{1}{2} V^T Q V \\ s.t. \ & A_{\text{eq}} V = b_{\text{eq}} && \text{(32a)} \\ & A_{\text{ineq}} V \leq b_{\text{ineq}}, && \text{(32b)} \end{aligned}$$

From Assumptions 1, Problem (32) has a finite solution for any Q because the feasibility domain is bounded and not empty. The value of Q will be selected later. We use this problem to find a solution to (27a)-(27f). KKT is a necessary optimality condition for problems with linear constraints (Theorem 5.1.3 in [12]), therefore, there exist $V^\star$, $\mu^\star$, $\lambda^\star$ which satisfy the KKT conditions

$$A_{\text{eq}}^T \mu^\star + A_{\text{ineq}}^T \lambda^\star + Q V^\star = 0 \tag{33a}$$
$$A_{\text{eq}} V^\star = b_{\text{eq}} \tag{33b}$$
$$A_{\text{ineq}} V^\star \leq b_{\text{ineq}} \tag{33c}$$
$$\lambda^\star \geq 0 \tag{33d}$$
$$\left(A_{\text{ineq}} V^\star - b_{\text{ineq}}\right)_i \lambda_i^\star = 0, \ i \in \mathcal{I}, \tag{33e}$$

where $\mu^\star$ and $\lambda^\star$ are the dual variables of the QP (32).

We choose Q and use $\mu^\star$, $\lambda^\star$ and $V^\star$ to compute $U^\star_{\text{eq}}$, $U^\star_{\text{ineq}}$, $I^\star_{\text{eq}}$ and $I^\star_{\text{ineq}}$

$$\begin{aligned} Q =& \operatorname{diag}\left(\mathbf{1}^T A\right) - A_{\text{eq}}^T \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right)^{-1} A_{\text{eq}} \\ & - A_{\text{ineq}}^T \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)^{-1} A_{\text{ineq}} && \text{(34a)} \\ I^\star_{\text{eq}} =& \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) \mu^\star && \text{(34b)} \\ U^\star_{\text{eq}} =& \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right)^{-1} A_{\text{eq}} V^\star - \mu^\star && \text{(34c)} \\ I^\star_{\text{ineq}} =& \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) \lambda^\star && \text{(34d)} \\ U^\star_{\text{ineq}} =& \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)^{-1} A_{\text{ineq}} V^\star - \lambda^\star. && \text{(34e)} \end{aligned}$$

Note that $\operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)$ and $\operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right)$ are invertible and positive from the assumptions of Lemma 1. Equations (34) are combined with (33) to obtain

$$\begin{aligned} & A_{\text{eq}} V^\star = \operatorname{diag}\left(\mathbf{1}^T A_{\text{eq}}^T\right) U^\star_{\text{eq}} + I^\star_{\text{eq}} && \text{(35a)} \\ & A_{\text{ineq}} V^\star = \operatorname{diag}\left(\mathbf{1}^T A_{\text{ineq}}^T\right) U^\star_{\text{ineq}} + I^\star_{\text{ineq}} && \text{(35b)} \\ & A_{\text{eq}}^T U^\star_{\text{eq}} + A_{\text{ineq}}^T U^\star_{\text{ineq}} = \operatorname{diag}\left(\mathbf{1}^T A\right) V^\star && \text{(35c)} \\ & A_{\text{eq}} V^\star = b_{\text{eq}} && \text{(35d)} \\ & A_{\text{ineq}} V^\star \leq b_{\text{ineq}} && \text{(35e)} \\ & I^\star_{\text{ineq}} \geq 0 && \text{(35f)} \\ & (A_{\text{ineq}} V^\star - b_{\text{ineq}})_i {I_{\text{ineq}}}^\star_i = 0,\ i \in \mathcal{I}. && \text{(35g)} \end{aligned}$$

Equations (35) have a solution and are identical to (31). Therefore, there exist $V^\star$, $U^\star$ and $I^\star$ solving (27a)-(27f) when $c = 0$. □

Our next goal is to show that there exists a U_{cost} such that the circuit solution is also a solution to the LP (1). To show this we make use of the LP dual problem [13]

$$\begin{aligned} & \max_{\lambda} \ b^T \lambda && \text{(36a)} \\ & \text{s.t. } [A_{\text{eq}}^T \ A_{\text{ineq}}^T]\lambda = c && \text{(36b)} \\ & \qquad \left[0 \ I_{|\mathcal{I}|}\right] \lambda \geq 0, && \text{(36c)} \end{aligned}$$

where $I_{|\mathcal{I}|}$ is an identity matrix of size equals to number of inequality constraints. We create the following feasibility problem

$$\begin{aligned} & \min_{\lambda, V} \ 0 && \text{(37a)} \\ & \text{s.t. } A_{\text{eq}} V = b_{\text{eq}},\ A_{\text{ineq}} V \leq b_{\text{ineq}} && \text{(37b)} \\ & \qquad [A_{\text{eq}}^T \ A_{\text{ineq}}^T]\lambda = c,\ \left[0 \ I_{|\mathcal{I}|}\right] \lambda \geq 0 && \text{(37c)} \\ & \qquad c^T V + b_-^T \lambda + b_+^T \lambda_- = 0,\ \lambda + \lambda_- = 0, && \text{(37d)} \end{aligned}$$

Figure 7: Circuit implementing the primal-dual feasibility problem (37). Primal and dual parts are connected via the zero duality gap constraint. For compactness, b_+ and b_- are represented as b and λ_- is part of λ.

where b_+ and b_- are the absolute values of the positive and the negative components of b, and λ_- equals to $-\lambda$. Note that in equation (37d) all coefficients are positive, and that (37d) is equivalent to $c^T V = b^T \lambda$. All feasible points of problem (37) are primal (1) and dual (36) optimal solutions [13].

Remark 6. *From the Assumption 3 and from the structure of* (37d)*, it follows that the matrix of equality and inequality constraints has non-negative coefficients and non-zero rows and columns.*

Problem (37) is solved by the circuit shown in Fig. 7. The circuit contains two parts: the primal circuit at the bottom and the dual circuit in the upper part. Primal and dual circuits have the form described in Fig. 5 and consist of equality and inequality sub circuits, corresponding to primal and dual constraints, respectively. Note that the cost circuit is not present in the primal and in the dual circuit. Instead, the primal and dual circuits are connected by an equality sub circuit that corresponds to the zero duality gap constraint (37d).

Proposition 1. *Let Assumptions 1-3 hold. The circuit in Fig. 7 admits a solution. Moreover, at any circuit solution, the voltages V^* of the variable nodes are a solution to the original LP* (1)*.*

Proof. The circuit in Fig. 7 consists only of equality and inequality sub circuits. As shown in sections 3.1 and 3.2 the variable nodes voltages must satisfy the associated equality or inequality constraints and thus equations (37). The feasible set of problem (37) is the set of all primal optimal and dual optimal variables of problem (1). This feasible set is bounded by assumption. This fact and the results from Remark 6 imply that all the assumptions of Lemma 1 are satisfied. We conclude that the circuit admits a solution. Moreover, every solution must be a solution of the original LP (1), because it satisfies simultaneously dual and primal problems with zero duality gap [13]. □

In the circuit shown in Fig. 7, the dual and the primal circuits are connected with a single wire. We denote by U_{cost}^{crit} the voltage of this connection when the circuit settles.

Lemma 2 (Existence of U_{cost}^{crit})**.** *Let Assumptions 1-3 hold. Consider the circuit in Fig. 5 and its corresponding equations* (27)*. A solution V^* to* (27) *with $U_{cost} = U_{cost}^{crit}$ is an optimizer of the LP* (1)*.*

Proof. If a voltage equals to $U_{\text{cost}}^{\text{crit}}$ is applied externally to the wire that connects the primal and the dual parts (at point α in Fig. 7), we can remove the dual circuit without affecting the primal one. Therefore, the circuit in Fig. 5 admits the same solution as the primal circuit in Fig. 7. □

Figure 8: Subnetwork that connects cost node and node j, when the remaining resistors are assumed to be zero.

To complete the proof of Theorem 1 we need to show that for any voltage $U_{\text{cost}} \leq U_{\text{cost}}^{crit}$ the circuit will continue to yield the optimal solution. Assume that U_{cost} is perturbed by ΔU_{cost} from the value U_{cost}^{crit}. We denote perturbed values of variable voltages V as ΔV and perturbed values of the cost current I_{cost} as ΔI_{cost}. Next, we examine the Thevenin equivalent resistance [14] as seen from the cost node. Refer to Fig. 8 showing a subnetwork connecting a cost node and an arbitrary node j. We want to compute a lower bound on the equivalent resistance as seen from the cost node. To this aim, we conservatively assume that all other positive resistors in the network are zero, i.e. $R_{k,l} = 0, \forall k, l$ s.t. $k \neq j$. In this scenario, all the variable nodes have the same potential that equals to the potential U_j. This implies that the total resistance R_{total} which can be seen from the cost node is greater or equal to all the cost resistances in parallel. Therefore we have:

$$R_{\text{total}} \geq \frac{1}{\sum_{i=1}^{n} c_i}. \tag{38}$$

From (27g) follows that

$$c^T \Delta V = \left(\sum_{i=1}^{n} c_i \right) \Delta U_{\text{cost}} + \Delta I_{\text{cost}}. \tag{39}$$

Using the total equivalent resistance we know that

$$\Delta I_{\text{cost}} = -\frac{\Delta U_{\text{cost}}}{R_{\text{total}}}. \tag{40}$$

Combination of (39), (40) and (38) yields

$$\frac{c^T \Delta V}{\Delta U_{\text{cost}}} = \sum_{i=1}^{n} c_i - \frac{1}{R_{\text{total}}} \geq 0. \tag{41}$$

The equation (41) states that the change in cost value must have the same sign as the change in ΔU_{cost}. Therefore, when U_{cost} is decreased the cost must decrease or stay the same. However, the cost cannot decrease, since it is already optimal. Therefore the cost must remain constant, and the circuit holds solution to the problem (1) for any $U_{\text{cost}} \leq U_{\text{cost}}^{crit}$. This result completes the proof of Theorem 1.

5. Dynamic Analysis of the LP Circuit

In the previous section we have shown that an equilibrium of the circuit in Fig. 5 is a solution to the LP problem (1). The next step is to analyze the stability of the equilibrium points under the presence of parasitic dynamic effects. This investigation is the subject of current ongoing research. Next we present two critical aspects which help understanding the dynamic properties of the proposed circuit.

Figure 9: N-port resistor network with ports U_i. All $R_{i,j}$ are positive resistances, all R_k are negative resistances.

Figure 10: Subnetwork that connects nodes i and j, after assuming that all other resistors are zero.

5.1. Circuit passivity

We are interested in showing that the general circuit in Fig. 5 is passive. We examine an N-port resistor network which includes all positive and negative resistors of the original circuit shown in Fig. 5, and ignores the diodes and the constant voltage sources. The resulting network is shown in Fig. 9.

Proposition 2 (Network non-negativity)**.** *The resistance network in Fig. 9 is equivalent to a resistance network with non-negative resistors.*

Proof. Our goal is to obtain a lower bound of an equivalent resistance between any two ports. From Fig. 9 we see that a sub-network that connects two ports consists of two negative resistances — one for each port, and a mesh of positive resistors between them. We want to find an equivalent resistance, that exist according to the Thevenin theorem [14]. Let U_i and U_j be the two nodes in question. Next, motivated by a fact that replacement of any of positive resistances with a zero resistance may only reduce the total equivalent resistance, we make a conservative assumption that all the resistors in this network, excluding resistors directly connected to negative resistors of the U_i and U_j nodes, are zero, thus $R_{k,l} = 0, \forall k, l$ s.t. $k \neq i, j$. In this case all variables nodes have the same potential. This sub-network is illustrated in Fig. 10. The equivalent resistance of this network is zero, since according to (6) the negative resistance is constructed to be equal to the negative of parallel combination of other node resistances. Therefore, the equivalent resistance between any two ports is at least zero. □

5.2. Parasitic Effects

The network in Figure 11 is a modification of the LP circuit Fig. 5 when the effect of parasitic wire capacitances are included in the model. The network has capacitors connected to all constraint nodes. The capacitors represent parasitic capacitance present in any real electric circuit. The circuit in Figure 11 can be seen as a switched linear system where the diode states define the system mode. The negative resistances present in the circuit can lead to circuit instability [15]. In particular, if the negative resistor has an infinite bandwidth, this circuit can be shown to be unstable. In practice, the time constants of the negative resistor is limited and can be seen as a tuning variable. One can use existing hybrid

Figure 11: LP Analog Circuit with Parasitic Capacitance

system theory and tools [16] to design a piece-wise linear stabilizing controller where the unknowns are the time constants of the circuit implementing the negative resistances.

6. Quadratic Programming Circuit

Consider the set $\mathcal{Q}^-$ of all positive definite strictly diagonally dominant matrices with negative off-diagonal terms:

$$\begin{aligned}\mathcal{Q}^- = \{Q : (Q \succ 0) \wedge (Q_{ii} > \sum_{j,j\neq i} \|Q_{ij}\|) \\ \wedge (Q_{ij} < 0 \text{ for } i \neq j)\},\end{aligned} \tag{42}$$

and consider the following strictly convex quadratic program (QP)

$$\begin{aligned}&\min_V \ \frac{1}{2} V^T Q V - d^T V \\ &s.t. \ A_{\text{eq}} V = b_{\text{eq}} \\ &\quad A_{\text{ineq}} V \leq b_{\text{ineq}},\end{aligned} \tag{43}$$

where $Q \in \mathcal{Q}^-$ and the matrices $A_{\text{eq}}, A_{\text{ineq}}$ and d are non-negative. Any strictly positive QP with a strictly diagonally dominant quadratic cost can be written in this form.

Remark 7. *The matrix Q resulting from the transformation of a generic QP in the form* (43) *with $Q \in \mathcal{Q}^-$ and A_{eq}, A_{ineq} and d non-negative, is not unique.*

6.1. Augmenting the LP Circuit to generate a QP Circuit

In Lemma 1 it was shown that the solution to equations (27) when $c = 0$ is equivalent to the solution of the QP

$$\begin{aligned}&\min_V \ \frac{1}{2} V^T Q_A V \\ &s.t. \ A_{\text{eq}} V = b_{\text{eq}} \\ &\quad A_{\text{ineq}} V \leq b_{\text{ineq}},\end{aligned} \tag{44}$$

$$Q_A = \text{diag}(\mathbf{1}^T A) - A^T \,\text{diag}\left(\mathbf{1}^T A^T\right)^{-1} A. \tag{45}$$

Next we prove that Q_A is positive semi-definite.

Lemma 3. *Let $A \in \mathbb{R}^{m\times n}$ and $c \in \mathbb{R}^n$ be non-negative, $\mathbf{1}^T A > 0$ and $\mathbf{1}^T A^T > 0$, then the matrix*

$$Q_A = \text{diag}(c^T + \mathbf{1}^T A) - A^T \,\text{diag}\left(\mathbf{1}^T A^T\right)^{-1} A \tag{46}$$

is positive semi-definite.

Proof. From the definition of Q_A (46), the diagonal element in row j of Q_A is

$$\begin{aligned} Q_{A_{jj}} &= c_j + \sum_i A_{ij} - \sum_i \frac{A_{ij}A_{ij}}{\sum_k A_{ik}} \\ &= c_j + \sum_i A_{ij}\left(1 - \frac{A_{ij}}{\sum_k A_{ik}}\right). \end{aligned} \tag{47}$$

The diagonal element $Q_{A_{jj}}$ is non-negative, since A is non-negative and $\frac{A_{ij}}{\sum_k A_{ik}} \leq 1$. The row sum of all off-diagonal elements is

$$\sum_{l,l\neq j} Q_{A_{jl}} = \sum_{l,l\neq j}\sum_i \frac{A_{ij}A_{il}}{\sum_k A_{ik}}. \tag{48}$$

The difference between the j-th diagonal element and the sum of all the off-diagonal elements of row j is

$$\begin{aligned} &c_j + \sum_i A_{ij}\left(1 - \frac{A_{ij}}{\sum_k A_{ik}}\right) - \sum_{l,l\neq j}\sum_i \frac{A_{ij}A_{il}}{\sum_k A_{ik}} \\ &= c_j + \sum_i A_{ij}\left(1 - \frac{A_{ij}}{\sum_k A_{ik}} - \frac{\sum_{l,l\neq j} A_{il}}{\sum_k A_{ik}}\right) = c_j. \end{aligned} \tag{49}$$

If $c > 0$, the matrix Q_A is strictly diagonally dominant. If $c \geq 0$, the matrix Q_A is diagonally dominant. The matrix Q_A has non-negative main diagonal elements (47). Therefore, Q_A is positive definite when $c > 0$ or positive semi-definite for $c \geq 0$. □

Let the problem (1) be augmented with a redundant constraint

$$a^T V < \infty \tag{50}$$

where $a^T \geq 0$ is a non-negative row vector. This constraint has no influence on the feasible set since redundant. It is implemented by connecting each variable node V_i with resistor $\frac{1}{a_i}$ to a common node. Since the constraint is always inactive, the diode is always in non-conducting mode. Therefore, there is no need to include the diode and the negative resistance in the circuit.

Define

$$A' = \begin{bmatrix} A \\ a^T \end{bmatrix}. \tag{51}$$

From (46) follows that

$$Q(A') = Q_A + \mathrm{diag}(a) - \frac{aa^T}{1^T a}. \tag{52}$$

If a has only two non-zero entries a_i and a_j, then $Q(A')$ is the sum of the quadratic term Q_A arising from the original constraints A and a matrix $\alpha_{ij}\Delta Q^{ij}$.

$\alpha_{ij}\Delta Q^{ij}$ has all zero elements with the exception of two diagonal elements (i,i) and (j,j) equal to $\frac{a_i a_j}{a_i+a_j}$ and two off-diagonal elements (i,j) and (j,i) equal to $-\frac{a_i a_j}{a_i+a_j}$.

In conclusion, by adding a redundant constraint in the circuit with only two non-zero entries a_i and a_j, one can modify the elements (i,i), (i,j), (j,i) and (j,j) of the quadratic cost as

$$Q(A') = Q_A + \alpha_{ij}\Delta Q^{ij} \tag{53a}$$

$$\Delta Q^{ij} = \begin{bmatrix} 0 & & & & \\ & 1 & & -1 & \\ & & 0 & & \\ & -1 & & 1 & \\ & & & & 0 \end{bmatrix}, \ i \neq j \tag{53b}$$

$$\alpha_{ij} = \frac{a_i a_j}{a_i + a_j} \geq 0. \tag{53c}$$

Our next goal is to prove that one can generate the diagonal terms independently from the off-diagonal.

We augment constraints in (1) with a redundant constraint (50) and an additional variable V_{n+1} wired to a constant voltage: $V_{n+1} = r_i$. Define

$$V' = [V, r_i]. \tag{54}$$

Let $a = [0 \dots 0 \ \alpha_{ii} \ 0 \dots 0 \ \alpha_{ii}]$ be a $n+1$ dimensional vector of all zeros with exception of α_{ii} at positions i and $n+1$. Then,

$$\begin{aligned} V'^T Q(A') V' &= V^T Q_A V + \frac{1}{2}\alpha_{ii}(V_i - r_i)^2 \\ &= \frac{1}{2}\alpha_{ii}V_i^2 - \alpha_{ii} r_i V_i + \frac{1}{2} r_i^2. \end{aligned} \tag{55}$$

In conclusion by adding a redundant constraint implemented as a resistor $R = \frac{1}{2\alpha_{ii}}$ between the variable node V_i and the constant voltage source r_i we modify the cost as follows. The term α_{ii} is added to the i-th diagonal element of Q_A and $\alpha_{ii} r_i$ is added to the i-th element of the linear cost term. We define

$$\Delta Q^{ii} = \begin{bmatrix} 0 & & 0 \\ & 1 & \\ 0 & & 0 \end{bmatrix} \tag{56a}$$

$$d^i = -\alpha_{ii} r_i \Delta d^i \tag{56b}$$

$$\Delta d^i = [0 \dots 0, 1, 0 \dots 0]^T \tag{56c}$$

where ΔQ^{ii} is a matrix with all zeros with exception of 1 at the (i,i) position, and Δd^i is a vector of all zeros with exception of 1 at the i-th position.

The last step is to prove that one can add a number of redundant rows a^T to the original matrix of equality and inequality constraints A and add constant voltage sources r_i so that any quadratic cost Q and linear cost d in (43) can be obtained. In this case the LP circuit in Fig. 5 formulated for the constraint set A' and with $c = 0$ will solve the QP problem (43).

The generic cost function which can be obtained by adding multiple redundant rows and constant voltage sources is

$$J = \frac{1}{2}V^T \left(Q_A + \sum_{i=1}^{N}\sum_{j=1}^{N} \alpha_{ij}\Delta Q^{ij} \right) V + \left(\sum_{i=1}^{N} \alpha_{ii} r_i \Delta d^i \right) V. \tag{57}$$

We want to prove that there exist scalars α_{ij} and r_i such that J is equal to the QP cost in (43). The matrices $Q_A \succeq 0$ and $Q \in \mathcal{Q}^-$ are given. We first find a scalar β "large enough" such that $\Delta Q = \beta Q - Q_A$ and $\Delta Q \in \mathcal{Q}^-$. Note that the minimizer of $\beta J = \beta \left(\frac{1}{2} V^T Q V + d^T V \right)$ is the same as of J.

Proposition 3. *Consider the QP* (43) *and the matrices* $Q_A \succeq 0$ *and* $Q \in \mathcal{Q}^-$. *Define* $\Delta Q = \beta Q - Q_A$, $\Delta Q \in \mathcal{Q}^-$. *There exist scalars* $\alpha_{ij} \geq 0$ *and* r_i *for* $i, j = 1, \ldots, n$ *such that*

$$\sum_{i=1}^{N}\sum_{j=1}^{N} \alpha_{ij}\Delta Q^{ij} = \Delta Q \tag{58}$$

$$\sum_{i=1}^{N} -\alpha_{ii} r_i \Delta d^i = \beta d, \tag{59}$$

where ΔQ^{ij} and Δd^i have been defined in (53) and (56), respectively.

Proof. We can the construct the matrix ΔQ by using linear combination of ΔQ^{ij}. Let ΔQ_{ij} be the element (i, j) of the matrix ΔQ. $\Delta Q_{ij} < 0$ for $i \neq j$ since $\Delta Q \in \mathcal{Q}^-$. We choose $\alpha_{ij},\ i \neq j$, such that $\alpha_{ij} = -\Delta Q_{ij} > 0$. The matrix F

$$F = \Delta Q - \sum_{i=1}^{N} \sum_{j=1, j\neq i}^{N} \alpha_{ij}\Delta Q^{ij} \tag{60}$$

is diagonal. From the structure of ΔQ^{ij} in (53b) we know that the diagonal elements of the sum are equal exactly to the row sum of the non-diagonal elements. The matrix ΔQ is strictly diagonally dominant, therefore, the diagonal elements of F are positive. We set $\alpha_{ii} = F_{ii} > 0$.

The i-th non-zero element of βd in (59) equals to $-\alpha_{ii} r_i$, where $\alpha_{ii} > 0$. In order to satisfy (59) we set $r_i = -\frac{\beta d_i}{\alpha_{ii}}$. □

In conclusion, the QP problem (43) can be implemented with the analog circuit in Figure 5 by using the procedure described in this section.

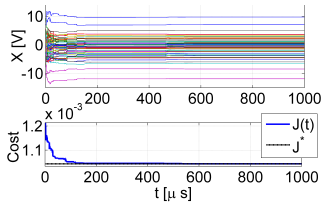

Figure 12: Example of LP solution. The upper plot shows solution variables in time. The lower plot shows the cost function value.

7. Simulations and Experiments

This section presents three examples where the approach proposed in this paper has been successfully applied. In the first example an LP is solved by the proposed electrical circuit simulated by using the SPICE [17] simulator. In the second example an analog LP is used to control a linear system by using Model Predictive Control. In the third example an experiment is conducted by realizing the circuit for a small LP with standard electronic components.

7.1. Linear Programming

We demonstrate capability of the method by solving an LP problem. The problem is a randomly generated and it has 120 variables, 70 equality constraints and 190 inequality constraints. In order to simulate parasitic effects of real circuit inductance values of $100nH$ are assumed for the wires, that roughly corresponds to inductance of 10 cm long wire.

The convergence of the electric circuit is shown in Fig. 12. The time scale in this example is determined by the selected value of parasitic inductance. The circuit transient can be partitioned to two phases. During the first $200\mu s$ rapid convergence to a solution close to the optimal one can be observed. Afterwards, at about $500\mu s$ the circuit converges to the true optimum value. Typical accuracy achieved in analog electronics is in the order of 0.5% of the dynamic range. The longer convergence time is not of practical interest, because the difference between the immediate cost value and the true optimal one is less than the accuracy that is expected from analog devices.

7.2. MPC example

This example demonstrates the implementation of a model predictive controller with an LP analog circuit. For this example we work with the dynamical system $\frac{dx}{dt} = -x + u$, where x is the system state and u is the input. We want x to follow a given reference trajectory, while satisfying input constraints. The

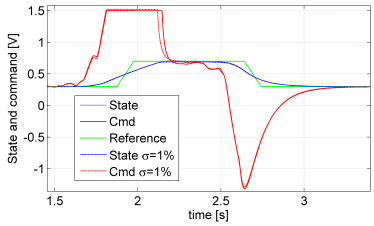

Figure 13: Example of MPC implementaion. Solid lines represent nominal controller, dashed lines represent controller implemented with random 1% error of analog devices.

finite time optimal control problem at time t is formulated as

$$\min_{u_0 \dots u_{n-1}} \sum_{i=1}^{N} |x(i) - x_{ref}(i)| \tag{61a}$$

$$x_{i+1} = x_i + (u_i - x_i)\delta, \ i = 0, \dots, N \tag{61b}$$

$$-1.5 \leq u_i \leq 1.5, \ i = 0, \dots, N \tag{61c}$$

$$x_0 = x(t) \tag{61d}$$

where N is the prediction horizon, $x_{ref}(i)$ is the reference trajectory at step i, δ is sampling time and $x(t)$ is the initial state at time t. Only the first input, u_0, is applied at each time step t.

With $N = 16$, the LP in (61) has 96 variables, 63 equality constraints and 49 inequality constraints. An electric circuit that implements system dynamics together with the circuit that implements the MPC controller were constructed and simulated using SPICE. The voltage value representing the system state was measured and enforced on the x_0 node of the LP. The optimal input value u_0 was injected as input to the simulated system dynamics. Fig. 13 shows the closed loop simulations results. Notice the predictive behavior of the closed loop control input and the satisfaction of the system constraints.

In order to demonstrate system performance for imperfect analog devices, another simulation result with 1% random Gaussian error in values of resistors is presented on the same Fig. 13. There is no significant change in system behavior.

7.3. Hardware implementation example

We implemented a small LP using standard electronics components. The same problem was realized by Hopfield [2] and Chua [3]. The LP is defined as follows

$$\begin{aligned} &\min_{x_1, x_2} c^T [x_1 \ x_2]^T \\ s.t. \ &\frac{5}{12} x_1 - x_2 \leq \frac{35}{12}, \quad \tfrac{5}{2} x_1 + x_2 \leq \tfrac{35}{2} \\ &-x_1 \leq 5, \qquad\quad x_2 \leq 5 \end{aligned} \tag{62}$$

Table 1: Experimental and theoretical results (in parenthesis) for LP solution.

cost direction	x1 (exact)	x2 (exact)
1 1	4.996 (5.0)	4.99 (5.0)
-1 1	7.002 (7.0)	5.005 (5.0)
-1 -1	-7.012 (-7.0)	-4.98 (-5.0)
1 0	6.976 (7.0)	0.005 (0.0)

where c is a cost vector, that is varied to get different solution points. The circuit was realized using resistors of 1% accuracy, operational amplifiers (OP27) for the negative resistance and comparator (LM311) together with the switch (DG201) to implement functionality of an ideal diode .

Various values for the cost function c and test results are summarized in Table 1. Table 1 shows that the experimental results are accurate up to 0.5%. The circuit reaches an equilibrium 6 μs after the cost voltage was applied. The convergence time is governed by a slew rate of the OP27 that is limited to 2.8 $V/\mu s$.

8. Conclusion

In this paper we presented an approach to design an electric analog circuit that is able to solve feasible Linear and Quadratic Programs. The method is used to implement and solve MPC based on linear programming. We present simulative and the experimental results that demonstrate the effectiveness of the proposed method.

The reported LP solution speed of 6 μs is faster than any result that was previously reported in the literature, and may be significantly decreased further by selecting faster components or implementing the design using faster technology, such as custom VLSI design or FPAA device.

Future research directions have interesting theoretical and implementations challenges. The theoretical aspects include analog complexity theory and the study the dynamic circuit behavior using the theory of Linear Complimentary system [18]. The implementations aspects includes solutions to the optimal circuit design, implementation using VLSI technologies and application to real-world problems.

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